library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity counter is

Port ( clk : in STD\_LOGIC;

rst : in STD\_LOGIC;

q : out STD\_LOGIC\_VECTOR (3 downto 0));

end counter;

architecture Behavioral of counter is

begin

process(clk,rst)

variable temp:std\_logic\_vector(3 downto 0);

begin

if(rst='1')then

temp:="0000";

elsif(clk'event and clk='1')then

temp:=temp+1;

end if;

q<=temp;

end process;

end Behavioral;

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY countertest IS

END countertest;

ARCHITECTURE behavior OF countertest IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT counter

PORT(

clk : IN std\_logic;

rst : IN std\_logic;

q : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

--Inputs

signal clk : std\_logic := '0';

signal rst : std\_logic := '0';

--Outputs

signal q : std\_logic\_vector(3 downto 0);

-- Clock period definitions

constant clk\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: counter PORT MAP (

clk => clk,

rst => rst,

q => q

);

-- Clock process definitions

clk\_process :process

begin

clk <= '0';

wait for clk\_period/2;

clk <= '1';

wait for clk\_period/2;

end process;

-- Stimulus process

stim\_proc: process

begin

-- hold reset state for 100 ns.

rst<='1';

wait for 100 ns;

rst<='0';

wait for 100 ns;

wait for clk\_period\*10;

-- insert stimulus here

wait;

end process;

END;

